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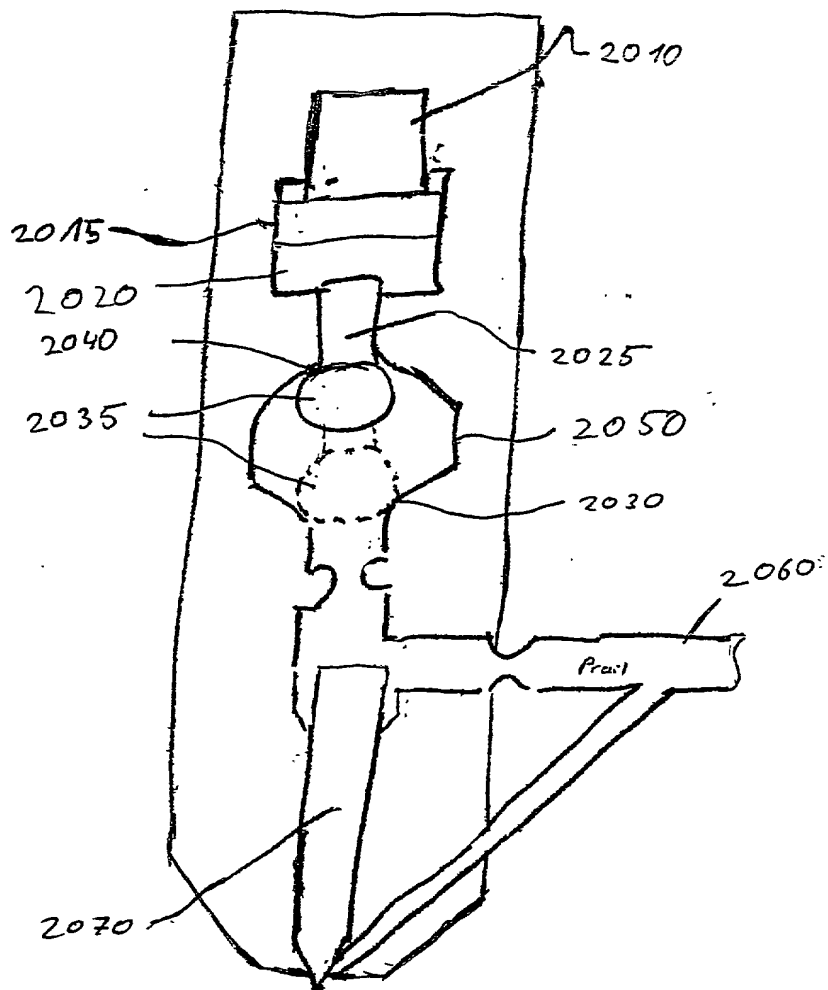
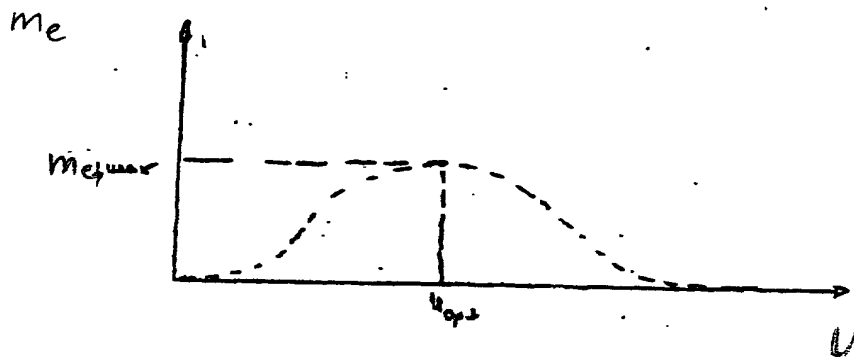


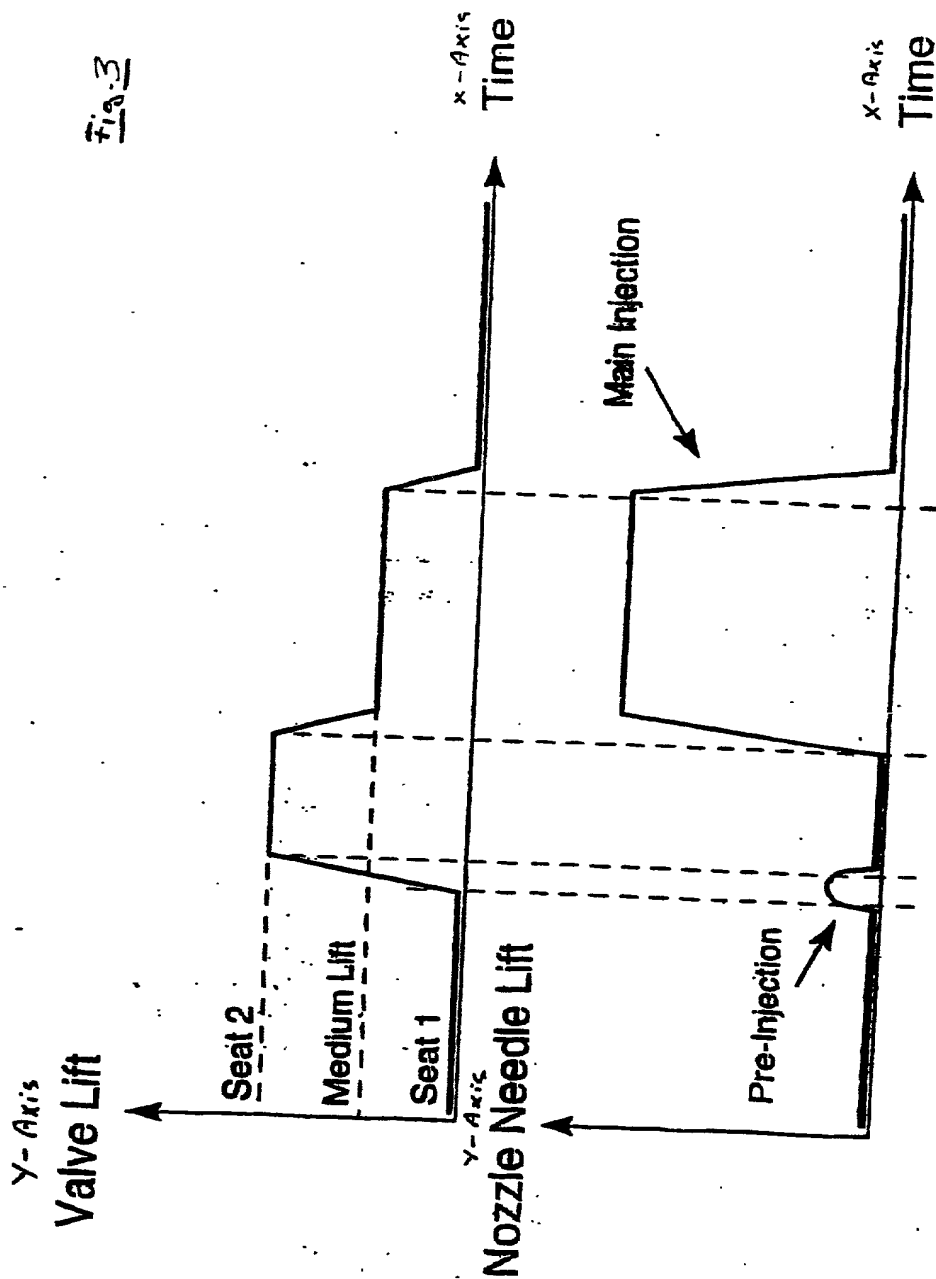
Fig. 7

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Fig-2



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[illegible]

FIG. 4

The diagram illustrates a semiconductor device, likely a memory array, with a grid of memory cells and peripheral control logic. The cells are organized into rows and columns, with word lines (10-15) and bit lines (20-25) intersecting. The peripheral logic includes sense amplifiers (61-65) and control circuitry (66-70). The device is shown in a cross-sectional view, with various layers and contacts labeled. The overall structure is a complex integrated circuit.

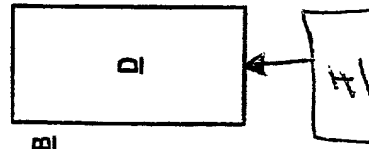


FIG. 5a

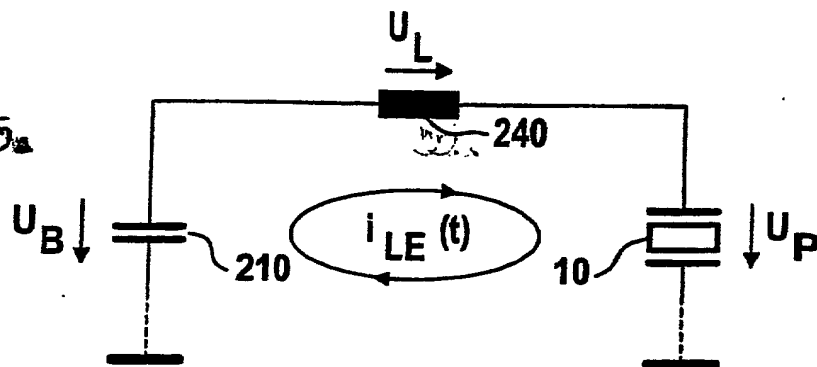


FIG. 5b

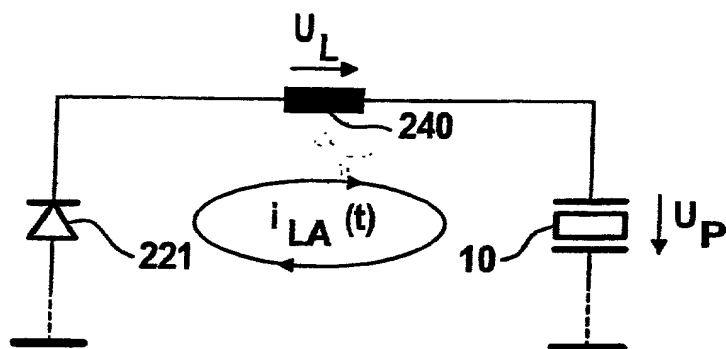


FIG. 5c

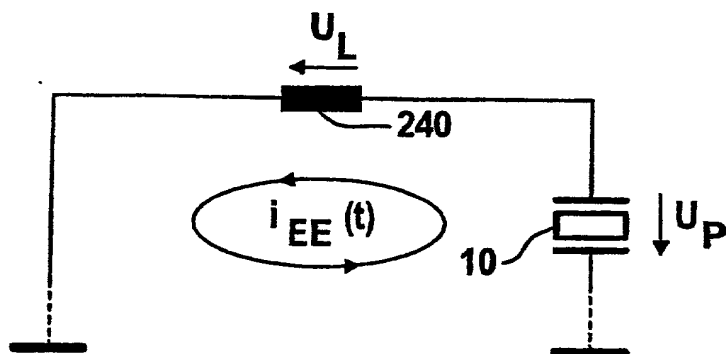
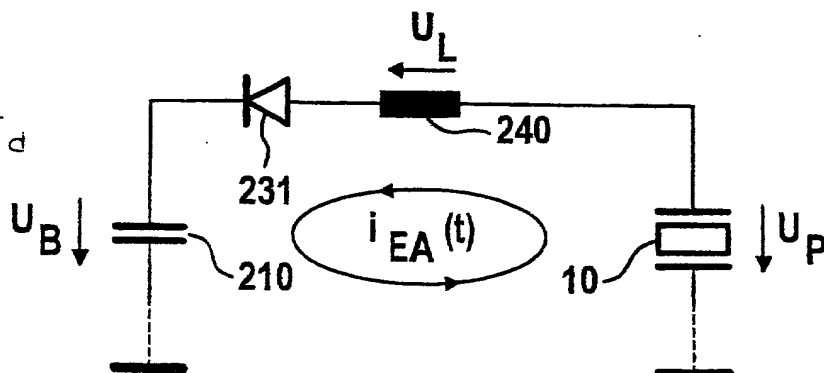


FIG. 5d



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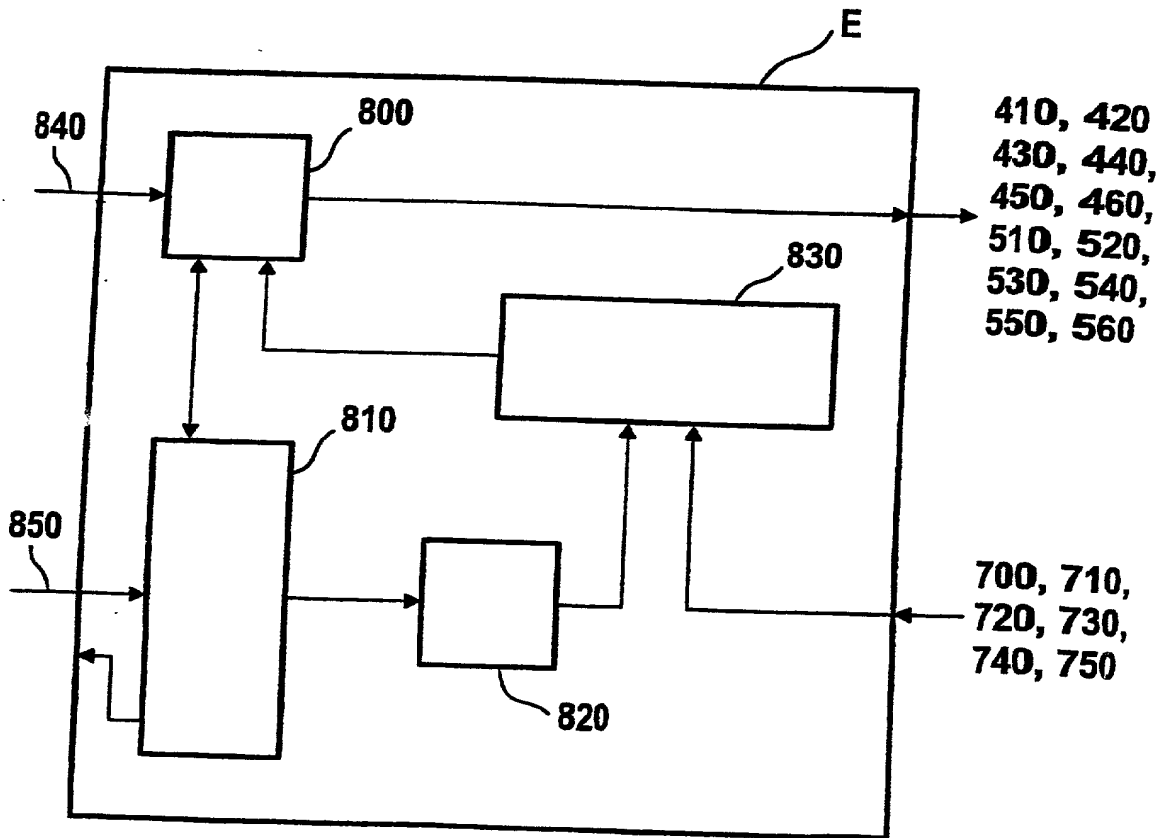


FIG. 6

Fig. 7

